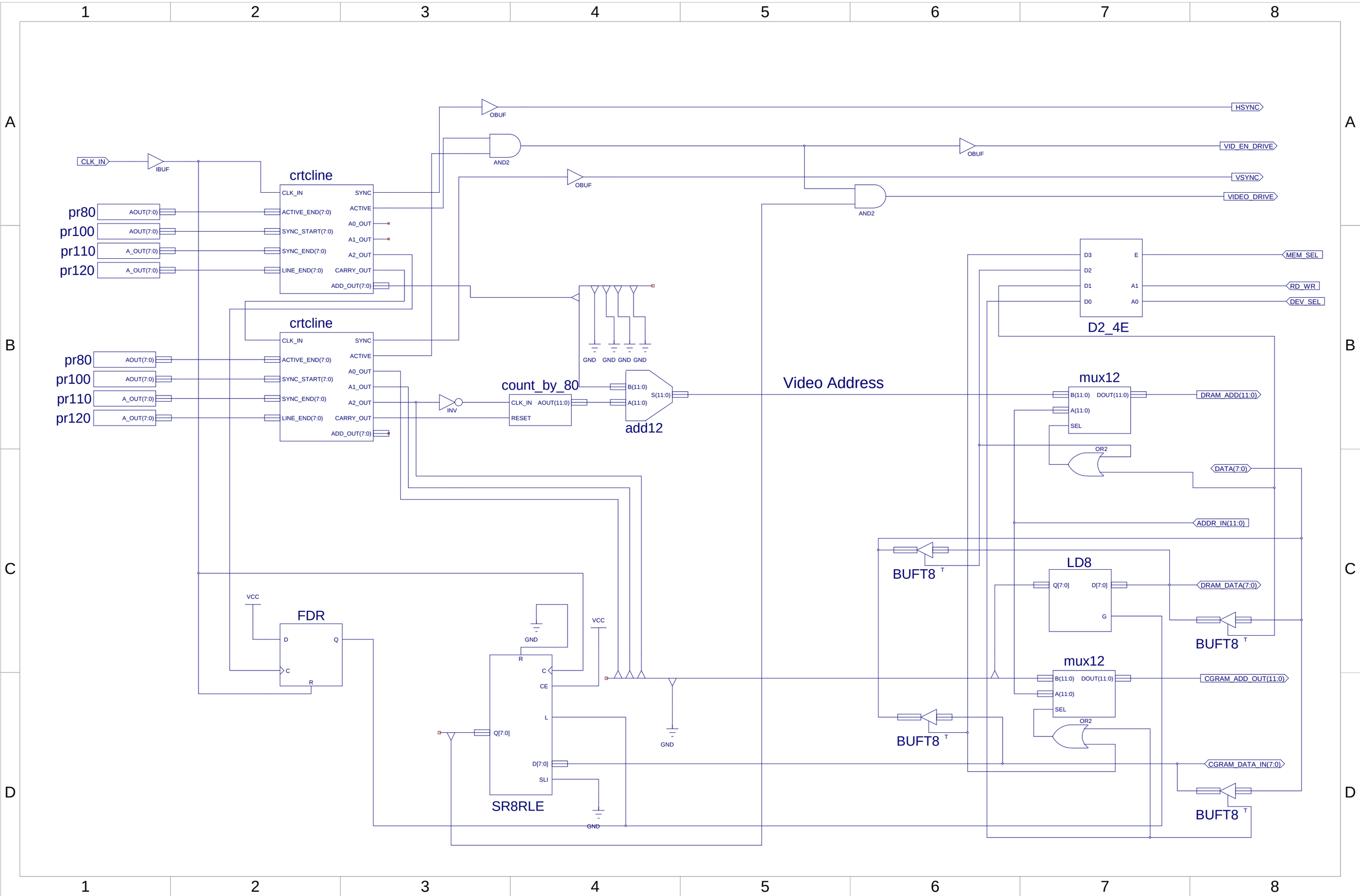
CLK_IN
IBUF
crtcline
CLK_IN
SYNC
ACTIVE_END(7:0)
ACTIVE
SYNC_START(7:0)
A0_OUT
A1_OUT
SYNC_END(7:0)
A2_OUT
LINE_END(7:0)
CARRY_OUT
ADD_OUT(7:0)
pr80
pr100
pr110
pr120
AOUT(7:0)
A_OUT(7:0)
crtcline
OBUF
AND2
HSYNC
VID_EN_DRIVE
VSYNC
VIDEO_DRIVE
GND
INV
count_by_80
CLK_IN
AOUT(11:0)
RESET
B(11:0)
A(11:0)
S(11:0)
add12
Video Address
D3
D2
D1
D0
E
A1
A0
D2_4E
MEM_SEL
RD_WR
DEV_SEL
mux12
B(11:0)
DOUT(11:0)
A(11:0)
SEL
DRAM_ADD(11:0)
OR2
DATA(7:0)
ADDR_IN(11:0)
BUFT8
LD8
Q[7:0]
D[7:0]
G
DRAM_DATA(7:0)
CGRAM_ADD_OUT(11:0)
CGRAM_DATA_IN(7:0)
VCC
FDR
D
Q
C
R
SR8RLE
CE
L
SLI